DESCRIPTION

The PT2465 is a PWM constant-current type stepping motor driver designed for sinusoidal-input micro-step control of stepping motors.

The PT2465 provides several excitation modes for bipolar stepping motor, such as 2-phase, 1-2-phase, W1-2-phase and 2W1-2 phase. The PT2465 is capable of forward and reverse driving of a 2-phase bipolar stepping motor using only a clock signal.

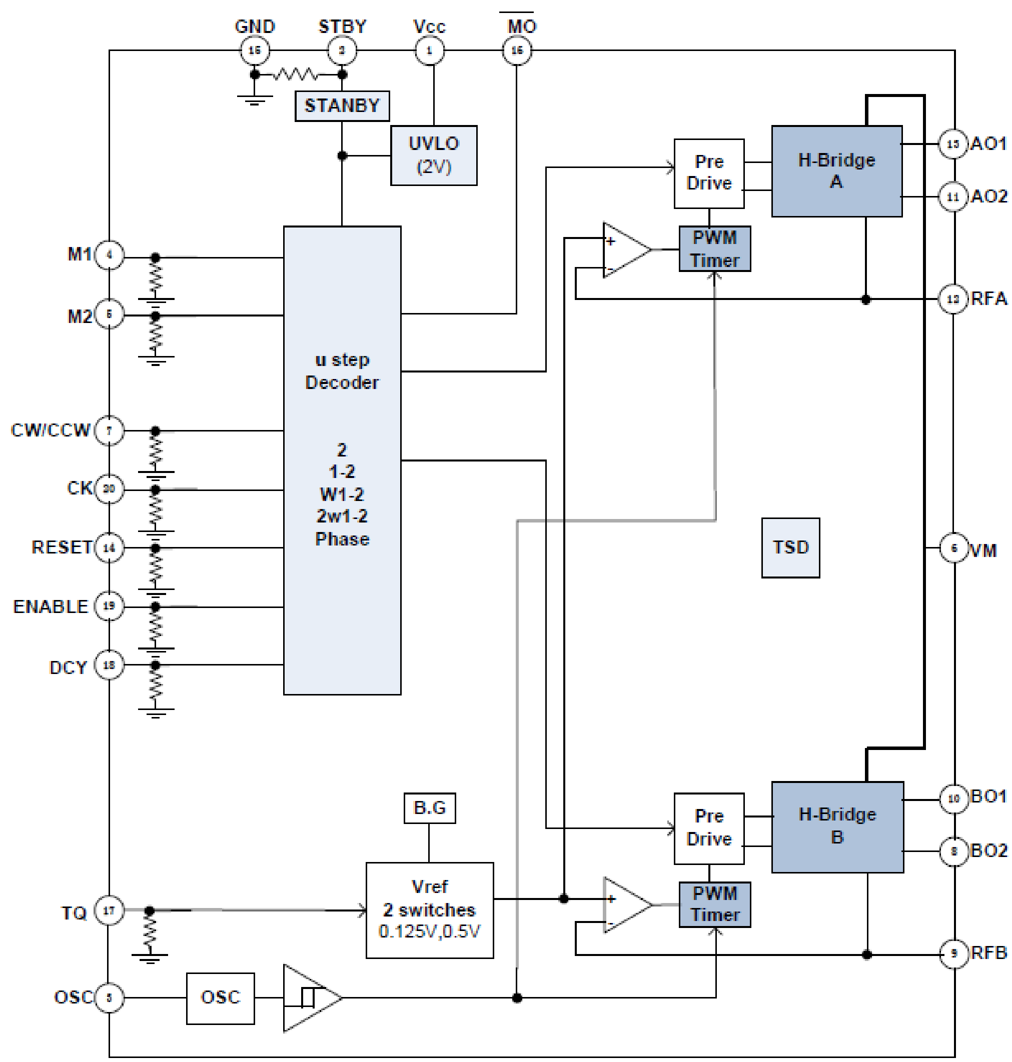
APPLICATIONS

- Digital camera system
- Interchangeable Lens

FEATURES

- Range of motor power supply voltage:
  - Control (VCC): 2.5V to 5.5V
  - Motor (VM) : 2.5V to 16V
- Output current: $I_{OUT} \leq 0.8$ A (max)
- Output ON-resistance: Ron = 1.5Ω (upper and lower total @VM = 7 V)
- Decoder that enables microstep control with the clock signal
- Selectable phase excitation modes (2, 1-2, W1-2 and 2W1-2)
- Internal pull-down resistors on inputs: 200 KΩ (typ.)
- Output monitor pin (MO)
- Thermal shutdown (TSD) protection
- Under voltage lock out (UVLO) protection
- Small surface-mount package (TSSOP-20 173mil, 0.65 mm lead pitch)

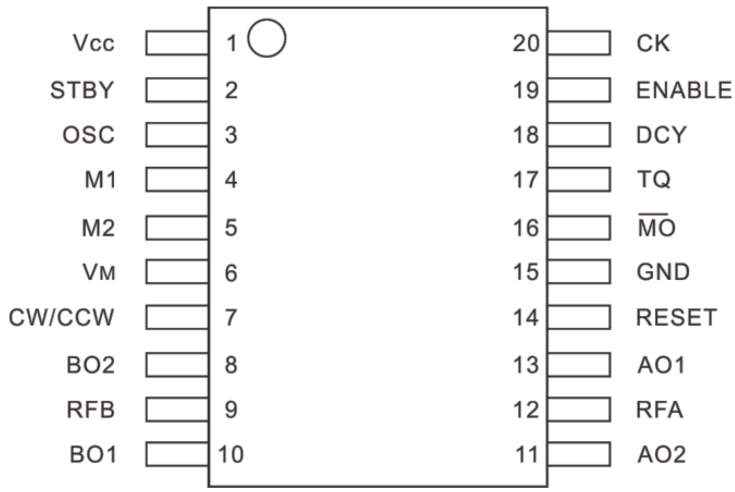
BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package Type	Top Code
PT2465	TSSOP 20, 173mil	PT2465

PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
V_{CC}	Power	Power supply pin for logic block	1
STBY	I	Standby input, See the Input Signals and Operating Modes table.	2
OSC	I	Connection pin for an external capacitor used for internal oscillation	3
M1	I	Excitation mode setting input 1, See the Excitation Mode Settings table.	4
M2	I	Excitation mode setting input 2, See the Excitation Mode Settings table.	5
V_M	Power	Power supply pin for output	6
CW/CCW	I	Rotation direction select input, See the Input Signals and Operating Modes table.	7
BO2	O	B-phase output 2, Connect BO2 to a motor coil pin.	8
RFB	O	Connection pin for a B-phase output current detection resistor	9
BO1	O	B-phase output 1, Connect BO1 to a motor coil pin.	10
AO2	O	A-phase output 2, Connect AO2 to a motor coil pin.	11
RFA	O	Connection pin for an A-phase output current detection resistor	12
AO1	O	A-phase output 1 Connect AO1 to a motor coil pin.	13
RESET	I	Reset input See the Input Signal and Operating Modes table.	14
GND	GND	Ground	15

MO	O	Monitor output, Initial state: MO = Low (open drain, pulled up by an external resistor)	16
TQ	I	Vref setting input See the Vref Voltage Setting table.	17
DCY	I	Decay setting input, See the Fast-Decay Time Inserted During the Current Decay Period table.	18
ENABLE	I	Enable input, See the Input Signal and Operating Modes table.	19
CK	I	Clock input	20

FUNCTIONAL TABLE

INPUT SIGNALS AND OPERATION MODES

Inputs					Operation Mode
CK	CW/CCW	RESET	ENABLE	STBY	
↑	L	H	H	H	CW
↑	H	H	H	H	CCW
X	X	L	H	H	Initial Mode
X	X	X	L	H	Enable Wait mode (Outputs: high impedance)
X	X	X	X	L	Standby mode (outputs: high impedance)

EXCITATION MODE SETTINGS

Inputs		Excitation Mode
M1	M2	
L	L	2-phase
H	L	1-2-phase
L	H	W1-2-phase
H	H	2W1-2-phase

INITIAL A- PAHSE AND B-PHASE CURRENT

(This table also applies to the currents on exit from standby mode.)

Excitation Mode	A-Phase Current	B-Phase Current
2-phase	100%	-100%
1-2-phase	100%	0%
W1-2-phase	100%	0%
2W1-2-phase	100%	0%

In this specification, the directions of current flows from AO1 to AO2 and from BO1 to BO2 are defined as the forward direction.

VREF VOLTAGE SETTING

Input	Vref
TQ	
L	0.125 V
H	0.5 V

SETTING THE CURRENT DECAY MODE

TABLE. FAST-DECAY TIME INSERTED DURING THE CURRENT DECAY PERIOD

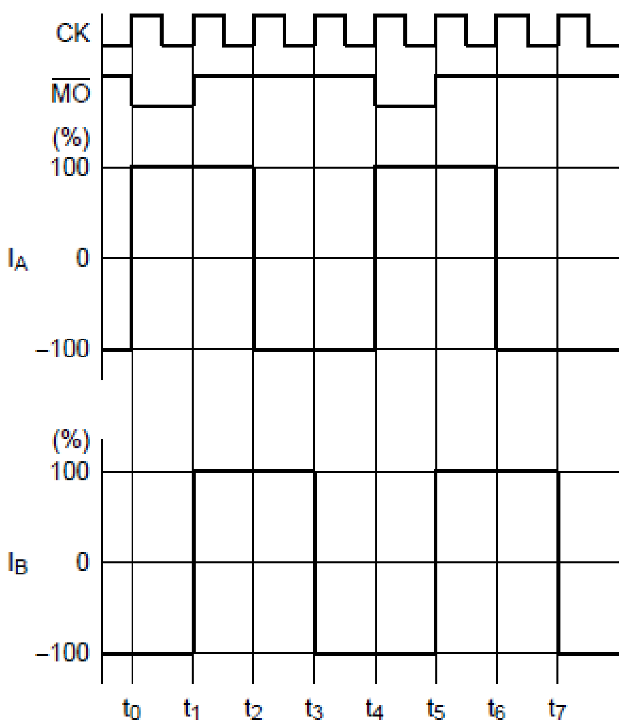
which is expressed as the number of CK cycles (an actual value may not exactly equal to the specified value)

Input	2W1-2phase			W1-2phase			1-2phase		
	Predefined Current	Number of CK Cycles		Predefined Current	Number of CK Cycles		Predefined Current	Number of CK Cycles	
DCY	%	TQ=H	TQ=L	%	TQ=H	TQ=L	%	TQ=H	TQ=L
L	100			100			100		
	98	0	0						
	92	0	0	92	0	0			
	83	0	0						
	71	0	0	71	0	0	71	0	0
	56	0	0						
	38	0	0	38	0	0			
	20	0	0						
	0	0	0	0	0	0	0	0	0
H	100			100			100		
	98	2	1						
	92	2	1	92	2	1			
	83	2	1						
	71	2	1	71	4	2	71	4	2
	56	4	2						
	38	4	2	38	4	2			
	20	4	2						
	0	0	0	0	0	0	0	0	0

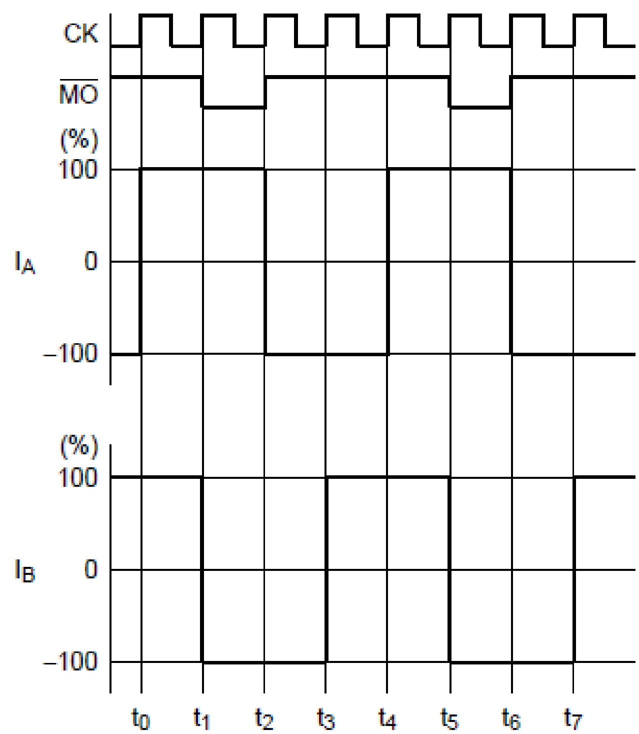
If no distortion can be observed in the output current waveform, the DCY pin should be kept high. The distortion reduction depends on the motor characteristics. If any distortion can be observed, the DCY pin should be kept low. Also, it should be ensured that the DCY input is set High only when the coil of a motor has an inductance of 1.5 mH or higher where fosc is no less than 100 KHz.

STEP CONTROL

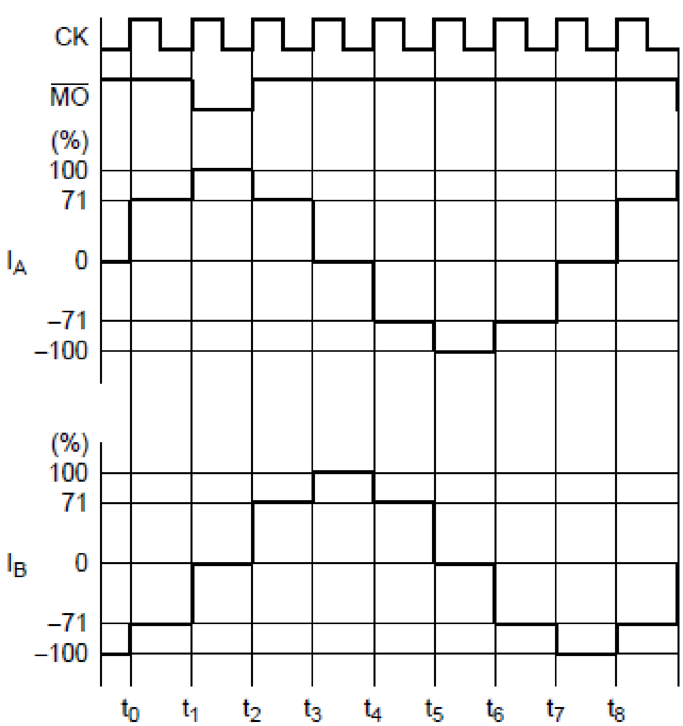
2-PHASE EXCITATION (M1, M2: L, L, CW MODE)



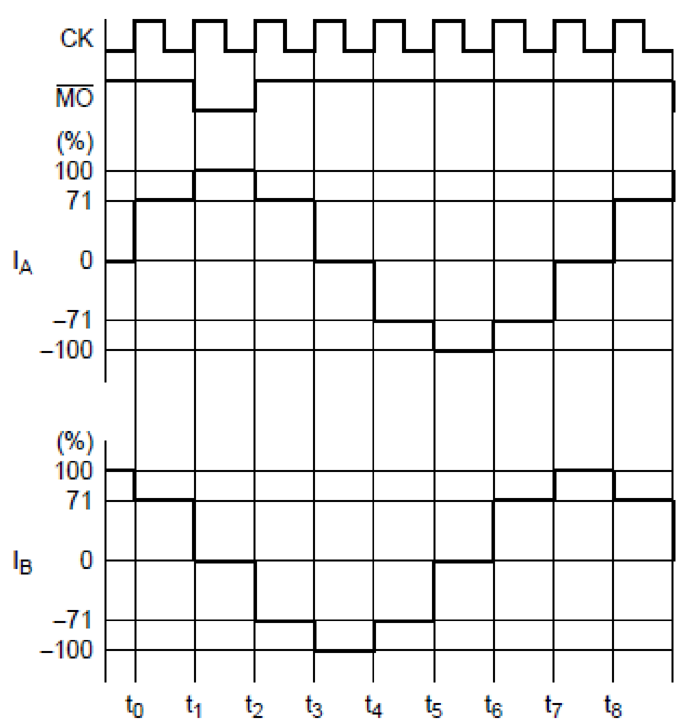
2-PHASE EXCITATION (M1, M2: L, L, CCW MODE)



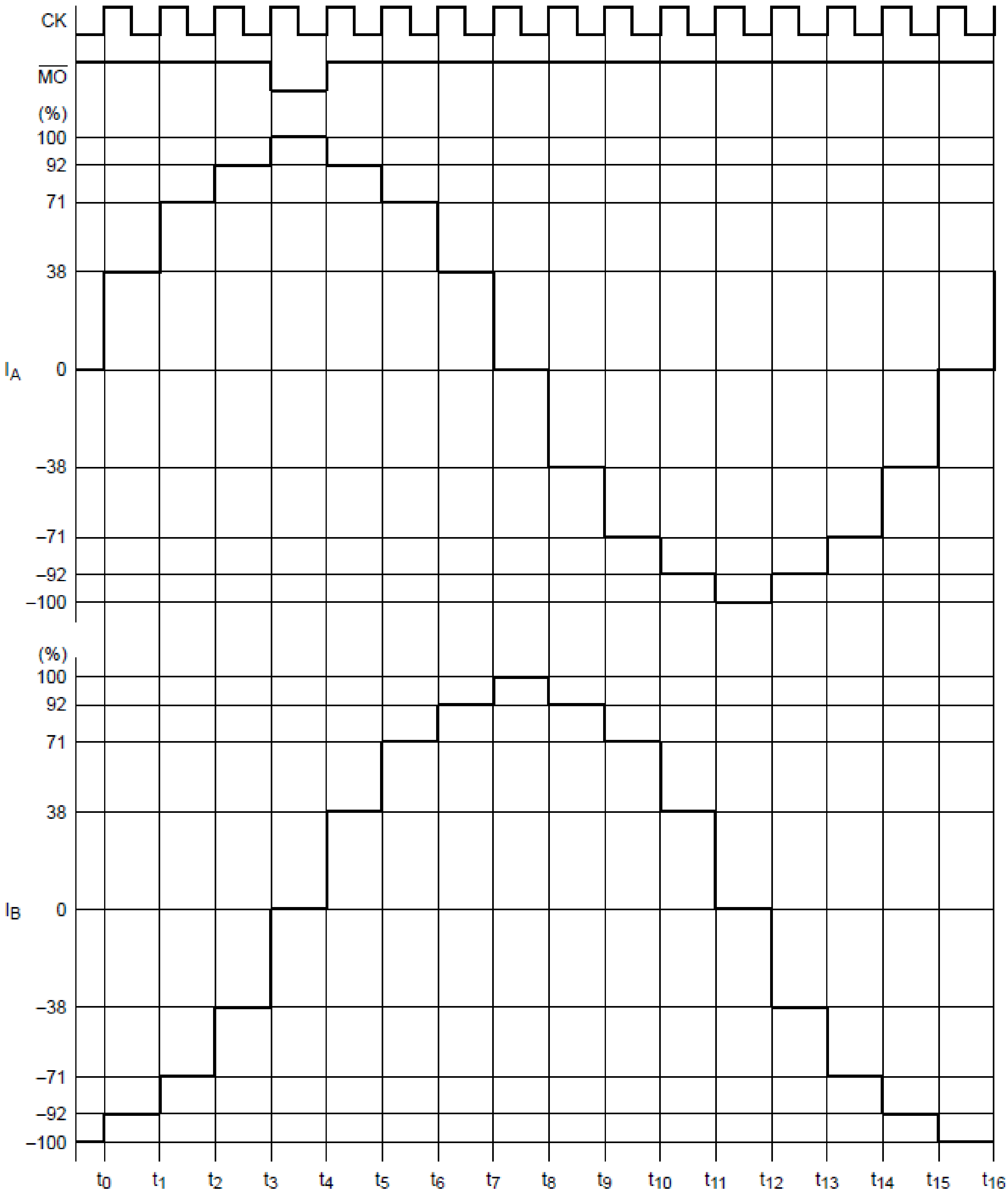
1-2-PHASE EXCITATION (M1, M2: H, L, CW MODE)



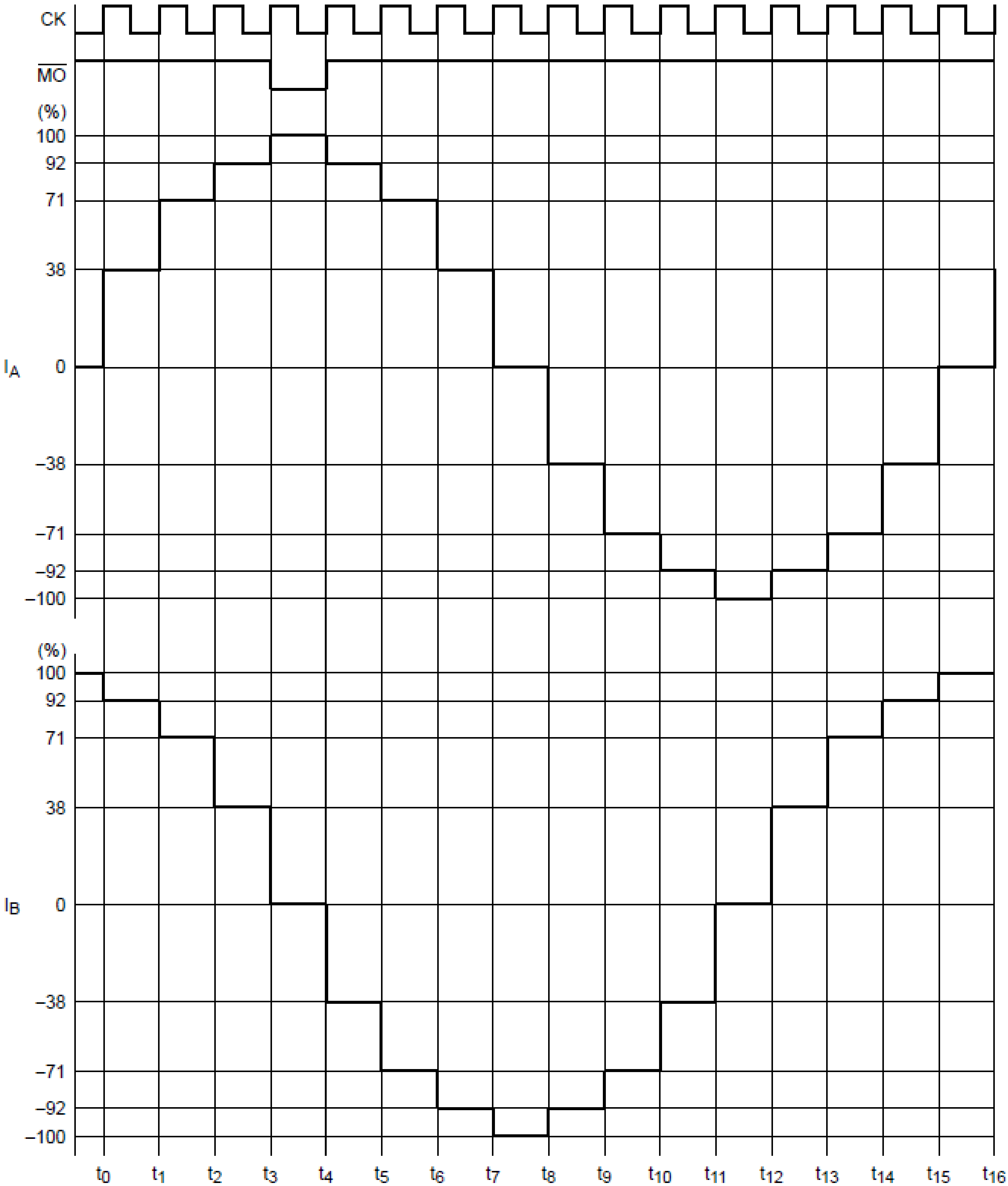
1-2-PHASE EXCITATION (M1, M2: H, L, CCW MODE)



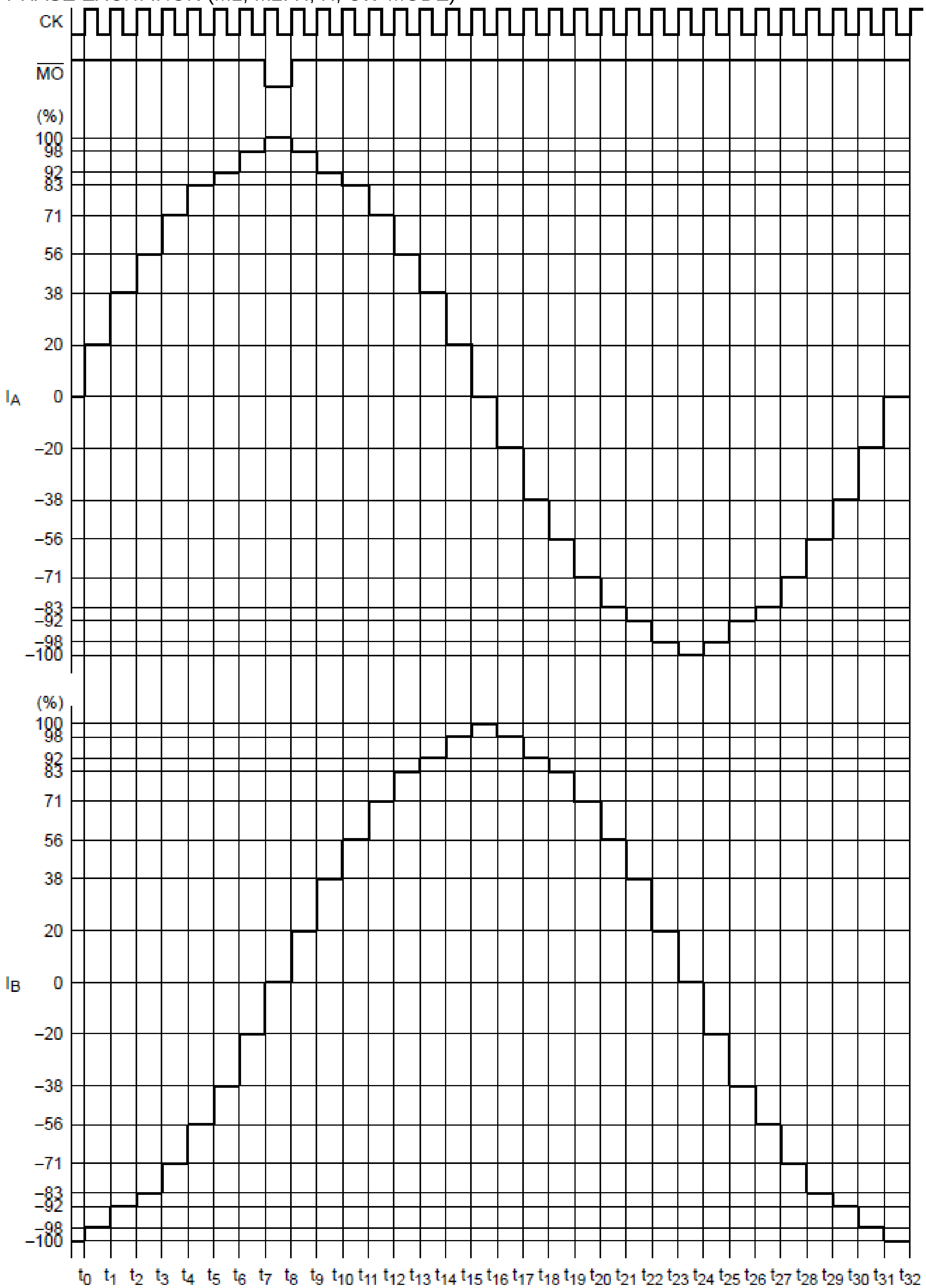
W1-2-PHASE EXCITATION (M1, M2: L, H, CW MODE)



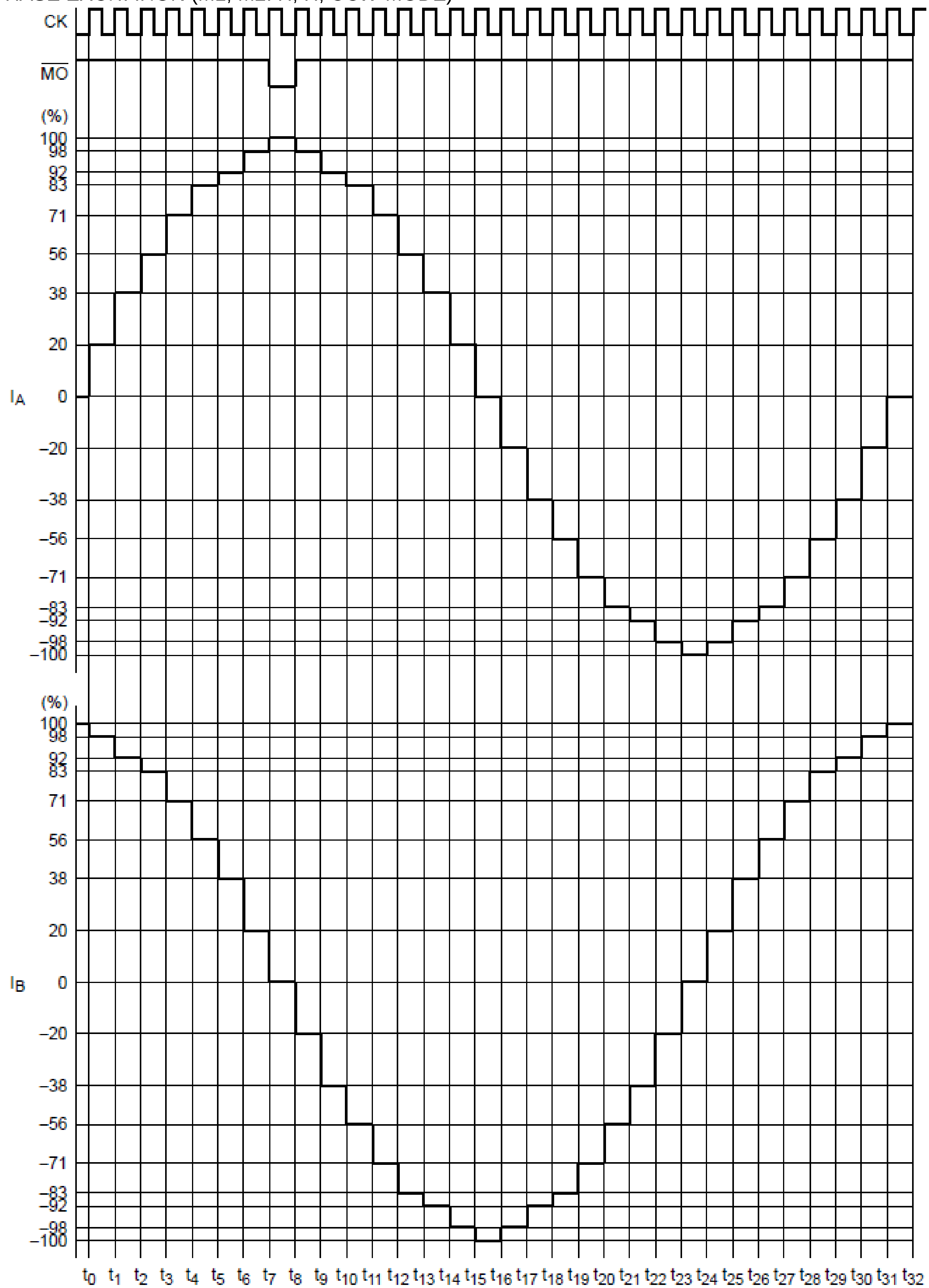
W1-2-PHASE EXCITATION (M1, M2: L, H, CCW MODE)



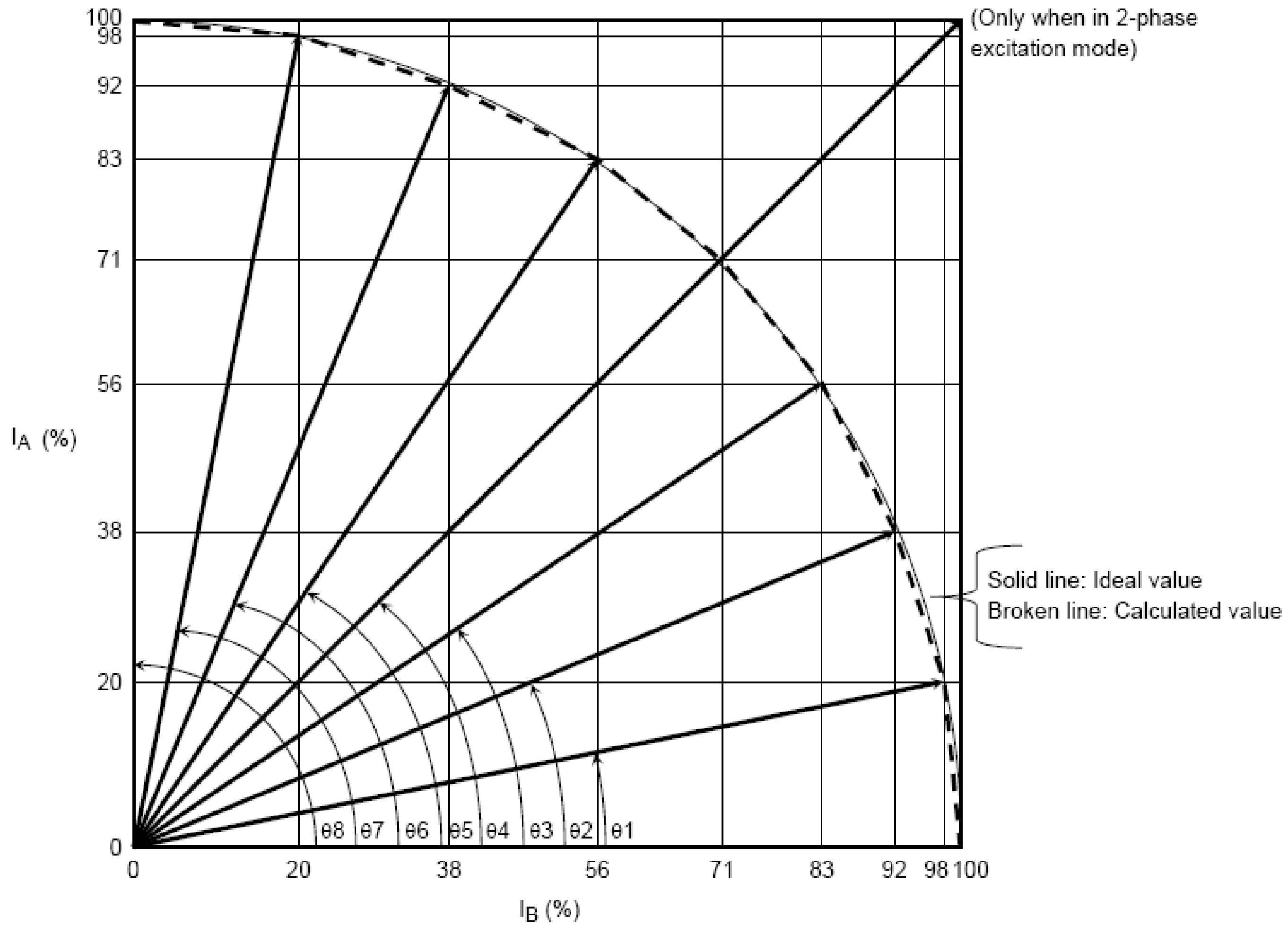
2W1-2-PHASE EXCITATION (M1, M2: H, H, CW MODE)



2W1-2-PHASE EXCITATION (M1, M2: H, H, CCW MODE)



OUTPUT CURRENT VECTOR LOCUS (NORMALIZING A SINGLE STEP TO 90 DEGREES)



θ	Rotation Angle		Vector Length		
	Ideal	Calculated	Ideal	Calculated	
θ0	0.000°	0.000°	100	100.00	-
θ1	11.250°	11.537°	100	100.02	-
θ2	22.500°	22.334°	100	99.54	-
θ3	33.750°	34.056°	100	100.12	-
θ4	45.000°	45.235°	100	100.41	141.42
θ5	56.250°	56.099°	100	100.12	-
θ6	67.500°	66.926°	100	99.54	-
θ7	78.750°	78.522°	100	100.02	-
θ8	90.000°	90.000°	100	100.00	-
			1-2-/W1-2-/2W1-2-phase		2-phase

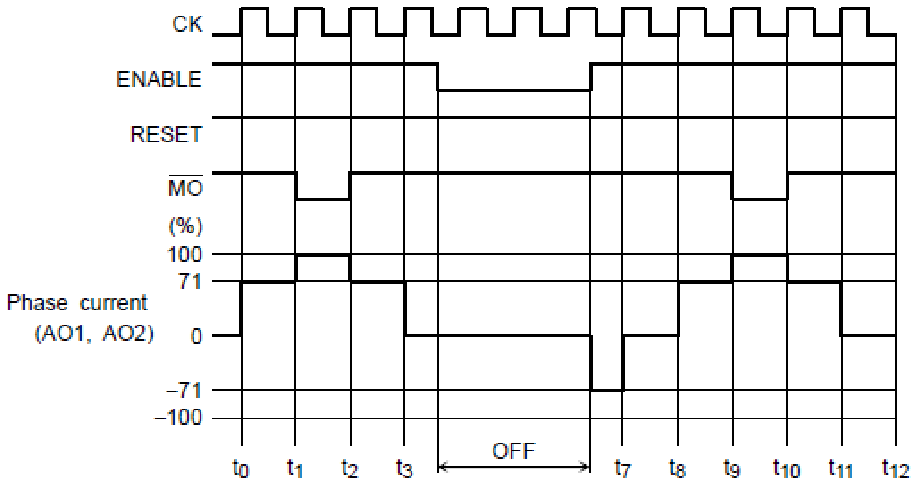
FUNCTION DESCRIPTION

RELATIONSHIP BETWEEN THE ENABLE INPUT AND THE PHASE CURRENT AND MO OUTPUTS

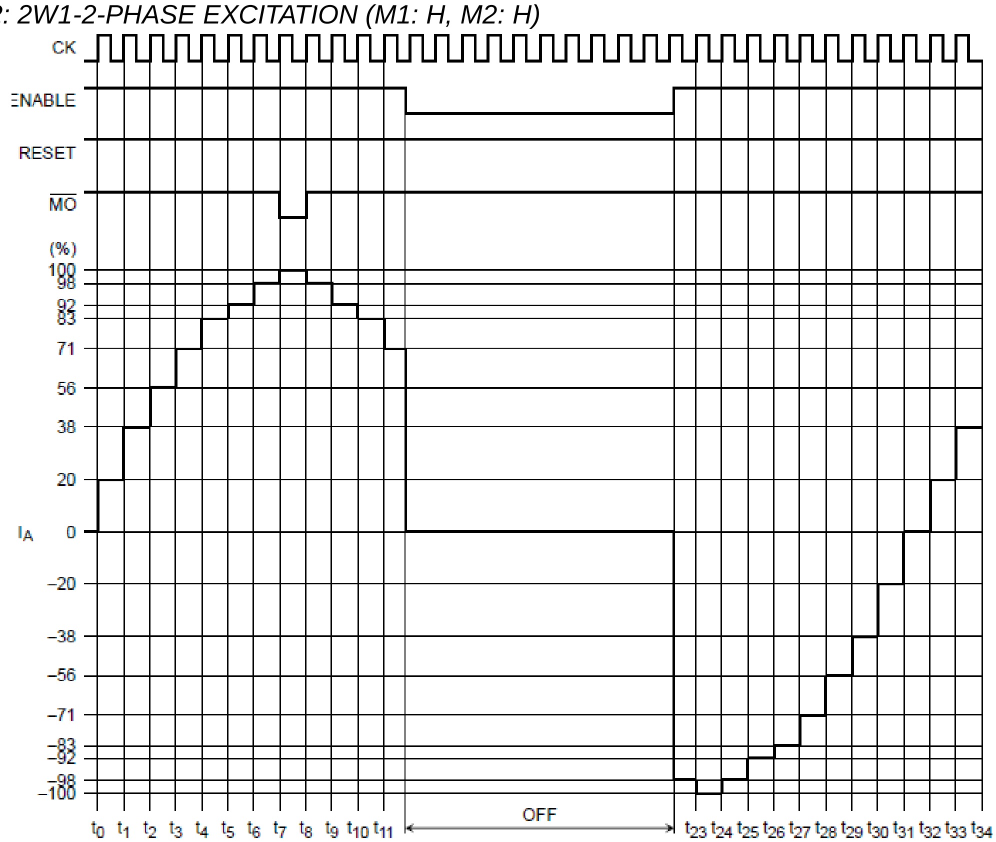
EXAMPLE 1: 1-2-PHASE EXCITATION (M1: H, M2: L)

Setting the ENABLE signal Low disables only the output signals. On the other hand, internal logic functions continue to operate in accordance with the CK signal.

Therefore, when the ENABLE signal goes High again, the output current generation is restarted as if phases proceeded with the CK signal.



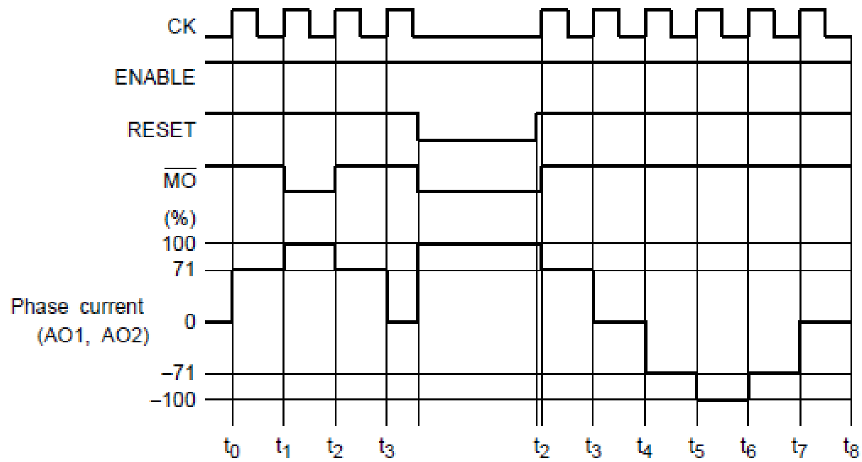
EXAMPLE 2: 2W1-2-PHASE EXCITATION (M1: H, M2: H)



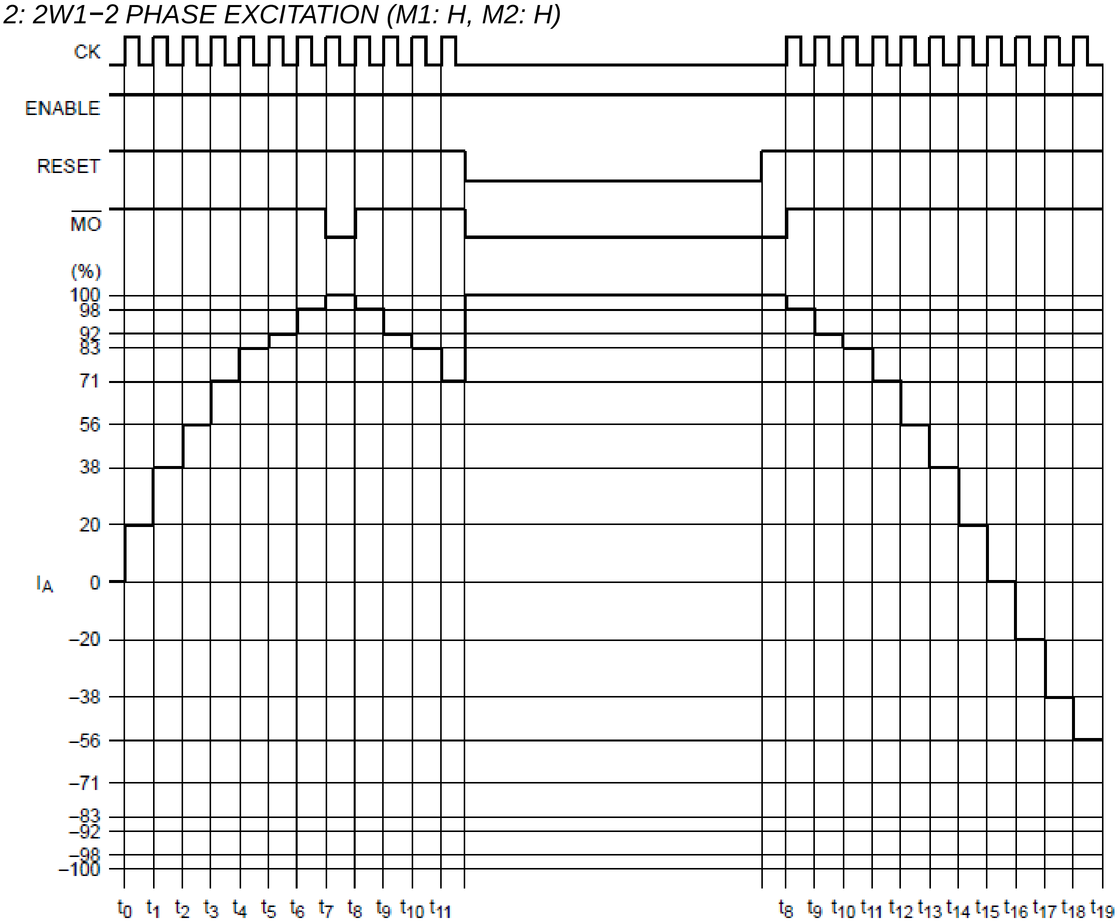
RELATIONSHIP BETWEEN THE RESET INPUT AND THE PHASE CURRENT AND MO OUTPUTS

EXAMPLE 1: 1-2-PHASE EXCITATION (M1: H, M2: L)

Setting the RESET signal Low causes the outputs to be put in the Initial state and the MO output to be Low. (Initial state: A-channel output current is at its peak (100%).) When the RESET signal goes high again, the output current generation is resumed at the next rising edge of the CK signal with the state following the Initial state. If RESET goes high when CK is already high, the output current generation is resumed immediately without waiting for the next rising edge of CK with the state following the Initial state.

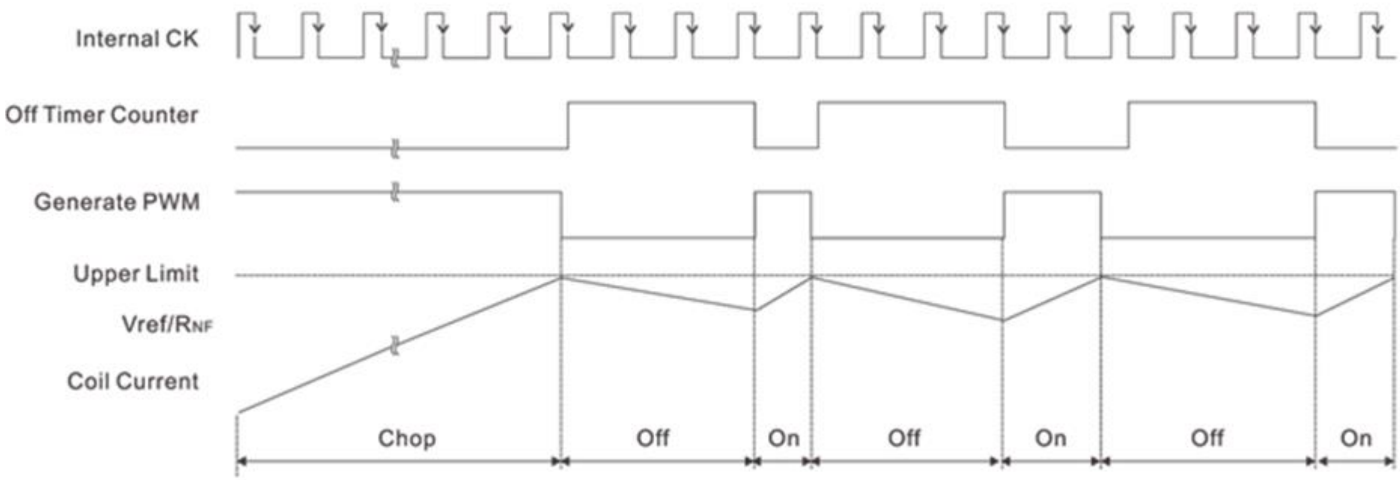


EXAMPLE 2: 2W1−2 PHASE EXCITATION (M1: H, M2: H)



CHOPPER CONTROL

Turning on the power (chop on) causes a current to flow into the coils. Once the V_{RF} voltage reaches Vref, it is detected by the comparator and the power is turned off (chop off).
The off timer/counter counts the number of falling edges of the internal CK signal, which is derived from the OSC signal, and generates the motor-driving PWM signal based on the turn-off time of four CK cycles.



The upper limit of the current across the motor coil (i.e., the peak current in each excitation mode), I (Limit), can be calculated as follows:

I (Limit) = Vref/R_{NF}

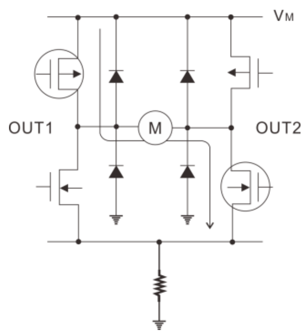
Vref equals to 0.125 V when TQ is Low, while it equals to 0.5 V when TQ is high.

R_{NF} is the value of resistors used for output current detection. One of those resistors is connected between R_{FA} and GND, and the other is connected between R_{FB} and GND.

Timing chart may be simplified for the sake of brevity.

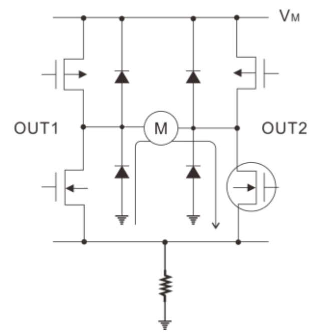
PWM CONTROL

In PWM mode, the motor operating mode changes between CW/CCW and short brake alternately.
To eliminate shoot-through current that flows from supply to ground due to the simultaneous conduction of high-side and low-side transistors in the bridge output, a dead time of 200 ns (design target value) is generated in the IC when transistors switch from on to off (t2), or vice versa (t4).
This permits a synchronous rectification PWM operation without controlling the dead time externally.



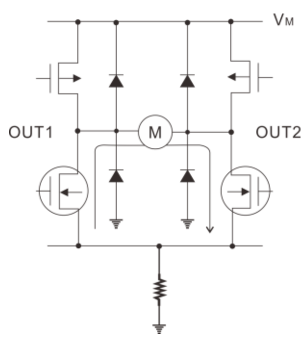
<PWM:ON> t1

→



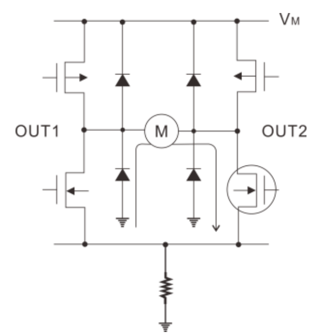
<PWM:ON→OFF> t2 = 200ns(typ.)

→



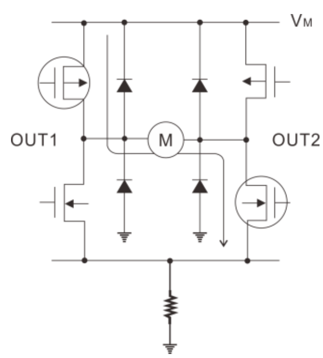
<PWM:OFF> t3

→

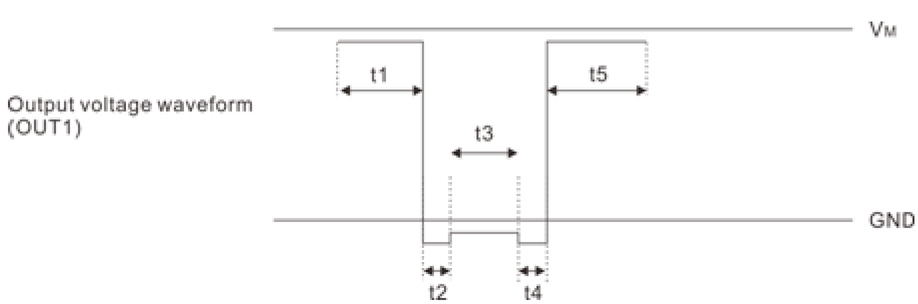


<PWM:OFF→ON> t4 = 200ns(typ.)

→

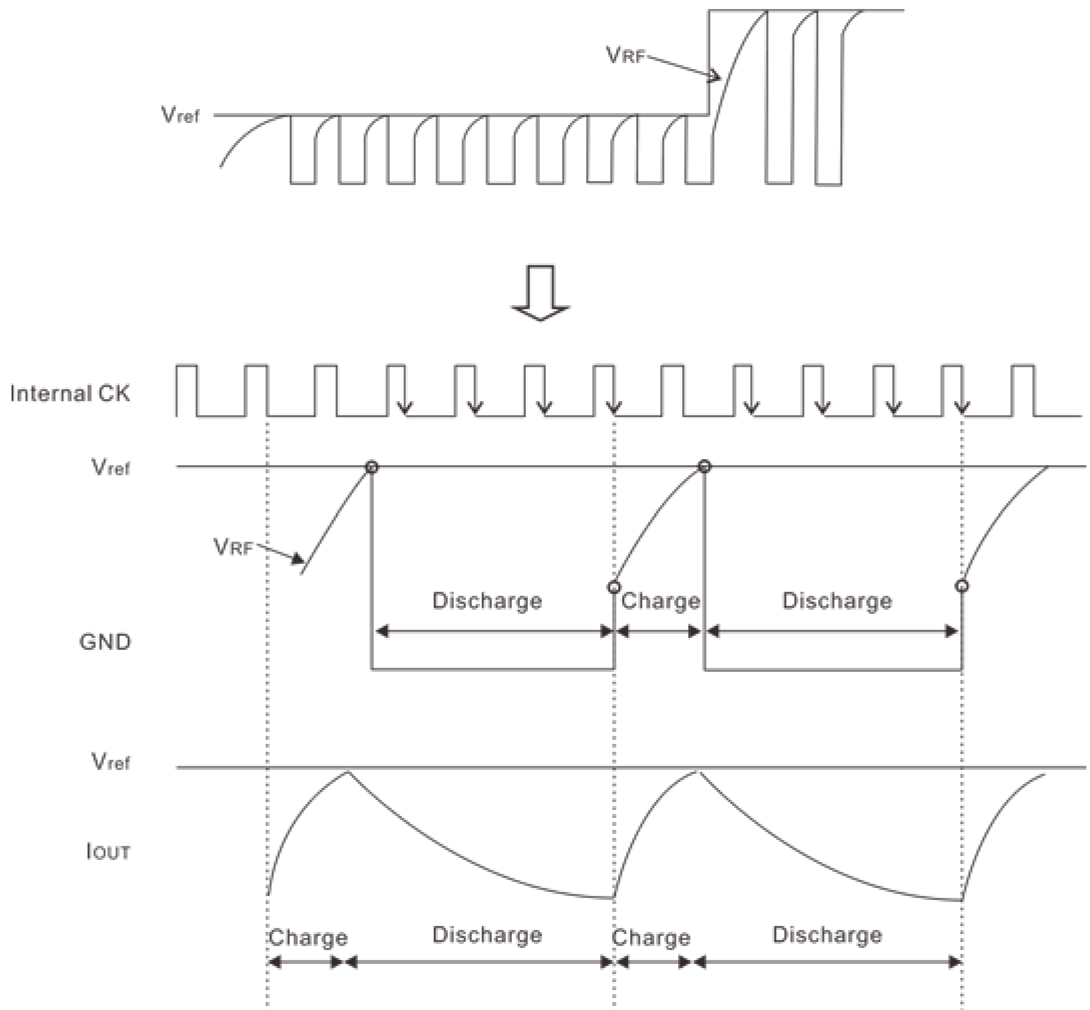


<PWM:ON> t5



1. CONSTANT-CURRENT CHOPPING

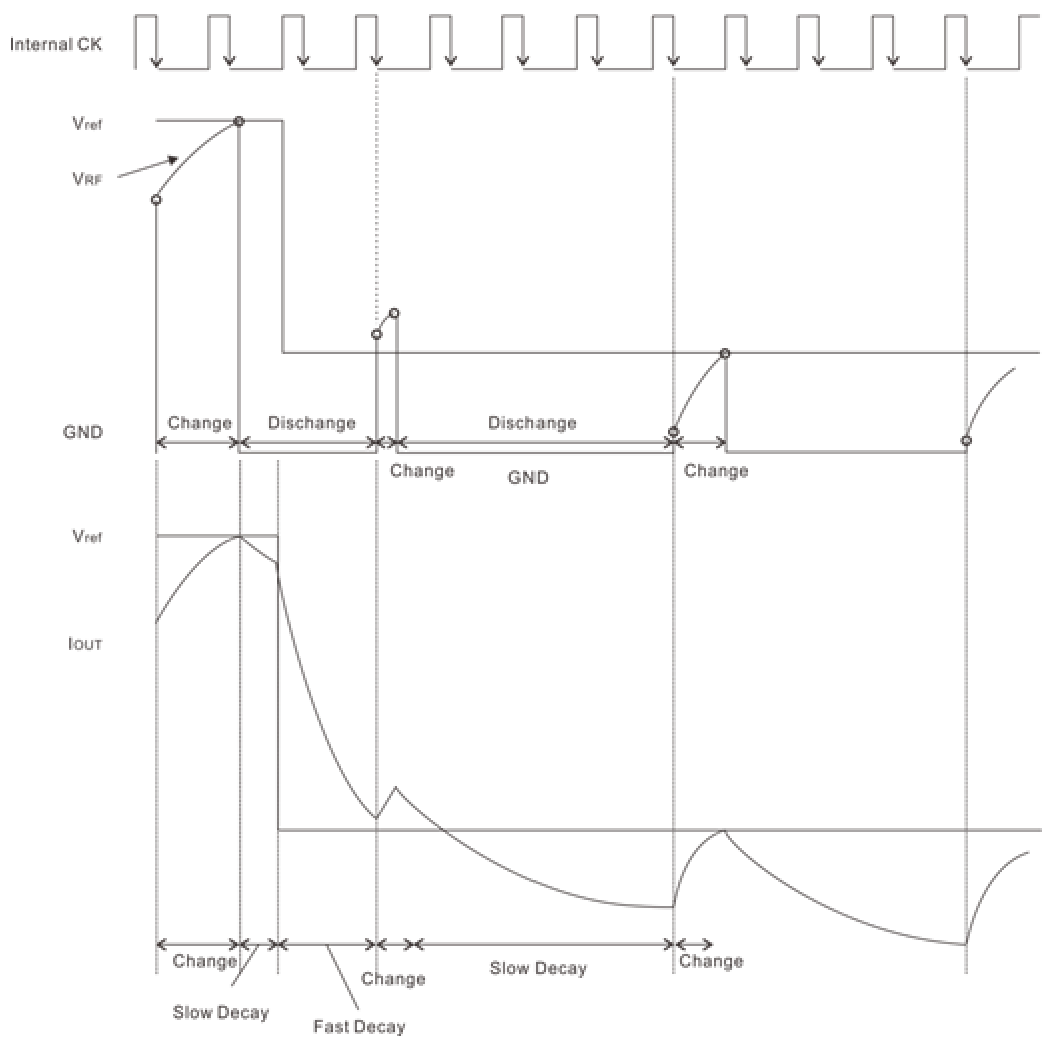
When V_{RF} reaches the predefined Vref voltage, the constant-current regulator enters Discharge mode.
After four cycles of CK, an internal clock generated by OSC, the regulator moves from Discharge mode to Charge mode.



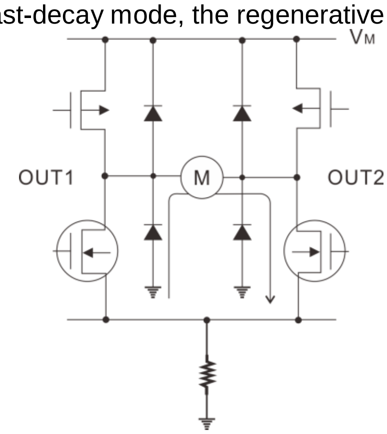
2. CHANGING THE PREDEFINED CURRENT TO THE LOWER VALUE

During deceleration, the regulator enters fast-decay mode immediately after the end of the current decay slope of slow-decay mode. The distortion of the current waveform can be reduced by the regenerative current from a coil that flows back to the power supply. Two CK cycles later, the regulator exits fast decay mode and enters Charge mode. (The fast-decay time, which is specified herein as two CK cycles, varies depending on the mode setting. A detailed description of the mode setting is provided in the Current Decay Mode section.)

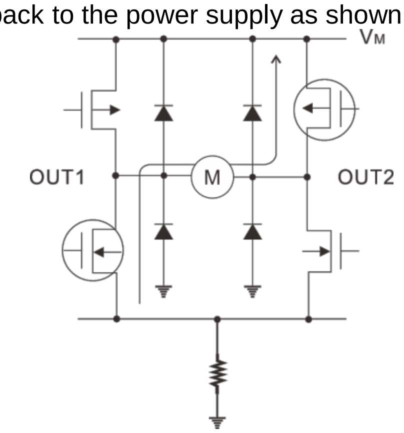
When V_{RF} reaches the reference voltage (Vref), the regulator enters Discharge mode. Four CK cycles later, the regulator exits Discharge mode and enters Charge mode. If V_{RF} > Vref when it enters Charge mode, however, it then reenters Discharge mode. Four CK cycles later, VRF is again compared against Vref. If V_{RF} < Vref, the regulator remains in Charge mode until VRF reaches Vref.



In fast-decay mode, the regenerative current from a coil flows back to the power supply as shown below.



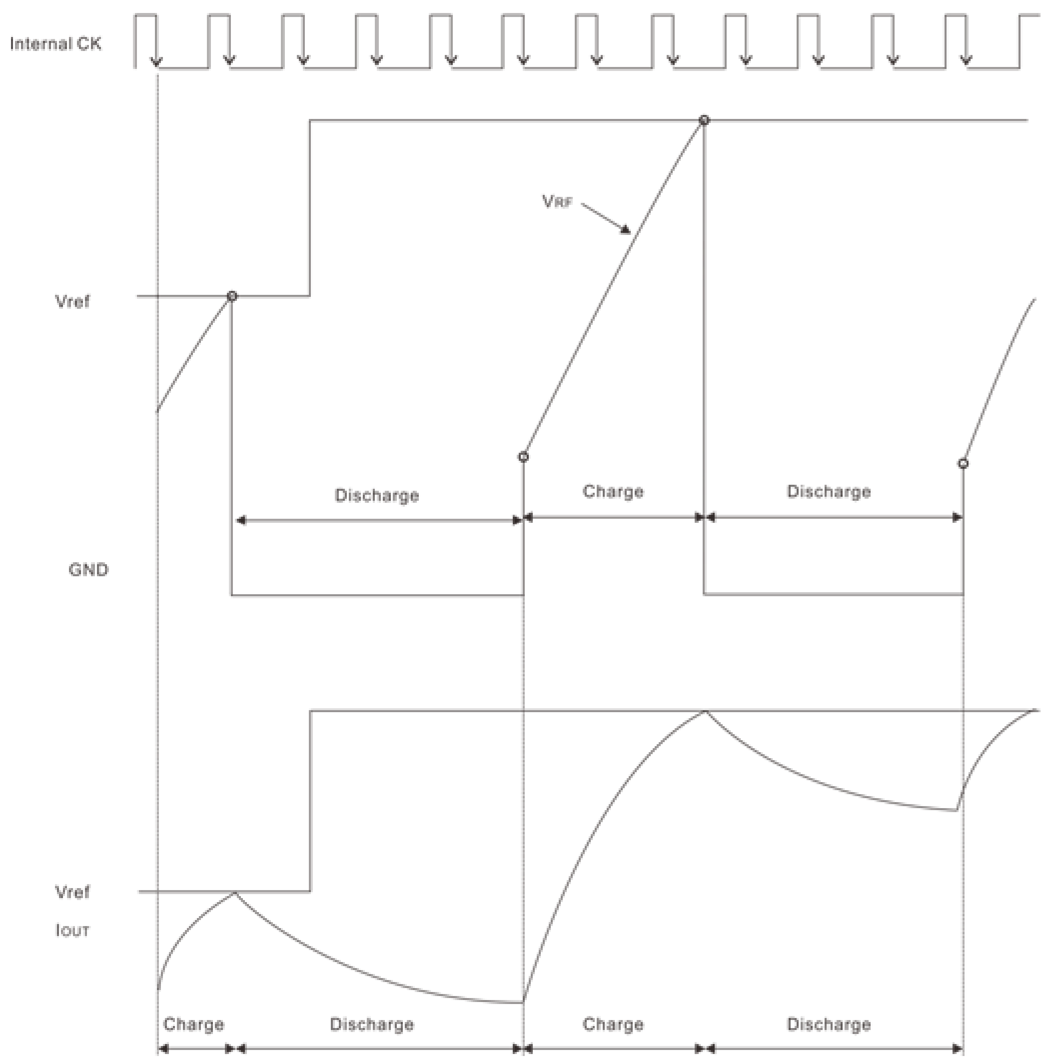
Slow Decay Mode



Fast Decay Mode

3. CHANGING THE PREDEFINED CURRENT TO THE HIGHER VALUE

Even when the Vref voltage is increased, the regulator remains in Discharge mode for four CK cycles and then enters Charge mode. During acceleration, the current decays only in slow-decay mode.



THERMAL SHUTDOWN (TSD) CIRCUIT

The PT2465 includes thermal shutdown protection circuit, which turns all of output driver off when junction temperature (Tj) exceeds 160℃ (typ.). After the junction temperature was cool down and Tj reaches the TSD hysteresis lowest window threshold, typically 40℃ below thermal shutdown did active, the output driver will automatically turn on.

TSD = 160℃ (design target value)
ΔTSD = 40℃ (design target value)

* In thermal shutdown mode, the internal circuitry and outputs assume the same states as in Enable Wait mode. Upon exit from thermal shutdown mode, they revert to those states which they assume when taken out of Enable Wait mode.

UNDER VOLTAGE LOCKOUT (UVLO) CIRCUIT

The PT2465 includes an under voltage lockout circuit, which puts the output transistors in the high-impedance state when V_{CC} decreases to 2.0 V (typ.) or lower. The output transistors are automatic turn on when V_{CC} increases past the lockout threshold, which is raised to 2.03 V by a hysteresis of 0.03 V.

Even when UVLO circuit is tripped, internal circuitry continues to operate in accordance with the CK input like when ENABLE is set Low. Thus, after the PT2465 exits the UVLO mode, the RESET signal should be asserted for putting the PT2465 in the Initial state if necessary.

ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Supply voltage	VCC		-0.3	6	V
	VM		-0.3	20.0	
Operating temperature	Topr		-20	85	℃
Storage temperature	Tstg		-40	150	
Maximum Power Dissipation	P_D	IC only		710	mW
		Mounted on $25cm^2$ PCB		960	
Output current	AO			0.8	A
	BO			0.8	
	MO			1	mA
Input voltage	Vi_{max}		-0.2	VCC+0.2	V
Output voltage	VMO		-0.2	VCC	V
ESD	HBM		3		KV
	CDM		0.75		KV
I/O Latch Up Current	I_{LU}		125		mA

RECOMMENDED OPERATING CONDITIONS (Ta=25℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power supply voltage	VCC	-	2.7	3.3	5.5	V
	VM	-	2.5	7	16	V
Output current	I_{OUT}	2.5 V < VM < 4.8 V	-	-	0.35	A
Output current	I_{OUT}	4.8 V < VM < 13.5 V	-	-	0.6	A
Input voltage	V_{IN}	-	-	-	V_{CC}	V
Clock frequency	f_{CK}	-	-	1	10	KHz
System frequency*	f_{SYS}	C_{OSC} = 220 pF	80	460	780	KHz
Chopping frequency	f_{CHOP}	-	20	115	195	KHz

Note:
The system frequency fsys can be calculated as follows :

$$\text{fosc} = \frac{I}{\Delta V_{OSC} \times C_{OSC}} = \frac{200uA}{1V \times C_{OSC}}$$

$$\text{fsys} = \text{fosc}/2$$

(Since this is an approximation formula, the calculation result may differ from the actual value.)

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, Ta=25℃, VCC=3.3V, VM=7V, R_{NF}=2Ω, C_{OSC}=220pF)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remark
Input voltage	$V_{IN(H)}$(1)	CW/CCW,CK,RESET ENABLE, M1, M2 (@V_{CC} = 3.3 V)	Vccx0.7	-	V_{cc}+0.2	V	Fig1
	$V_{IN(L)}$(1)		-0.2	-	0.8	V	
	$V_{IN(H)}$(2)	CW/CCW,CK,RESET ENABLE, M1, M2 (@V_{CC} = 5.5 V)	Vccx0.7	-	V_{cc}+0.2	V	
	$V_{IN(L)}$ (2)		-0.2	-	0.8	V	
	$V_{IN(H)}$ (3)	STBY, TQ, DCY	Vccx0.7	-	V_{cc}+0.2	V	
	$V_{IN(L)}$ (3)		-0.2	-	V_{cc}X0.15	V	
Input hysteresis voltage	V_H	CW/CCW,CK,RESET,ENABLE, M1, M2	-	150	-	mV	-
Input current	I_{INH}	V_{IN} = 3.0 V	5	15	25	μA	Fig1
	I_{INL}	V_{IN} = GND	-	-	1	μA	
Dynamic supply current	I_{CC1}	Outputs: Open, ENABLE: H, RESET H	-	1.7	2	mA	Fig2
	I_{CC2}	ENABLE: L	-	1.7	2	mA	
	I_{CC3}	Standby mode	-	-	1	μA	
	I_{M1}	Outputs: Open, ENABLE: H, RESET: H	-	300	500	μA	
	I_{M2}	ENABLE: L	-	300	500	μA	
	I_{M3}	Standby mode	-	-	1	μA	
Comparator reference voltage	$V_{RFA(1)}$ $V_{RFB(1)}$	TQ: L, 2-phase excitation	0.1	0.125	0.165	V	Fig3
	$V_{RFA(2)}$ $V_{RFA(2)}$	TQ: H, 2-phase excitation	0.445	0.5	0.555	V	
Channel-to-channel voltage differential	ΔV_O	B/A, TQ:L	-11	-	11	%	
Under voltage lock out threshold	Lower threshold	Output OFF	-		1.85	V	
	Upper threshold	Output ON	2.05		-	V	
MO output voltage	V_{MO}	I_{MO} = 1 mA	-	-	0.5	V	-
System frequency	f_{SYS}	C_{OSC} = 220 pF	300	460	620	KHz	-

This table shows which inputs are TTL-compatible and which ones are CMOS-Compatible. This also shows whether they are provided with hysteresis.

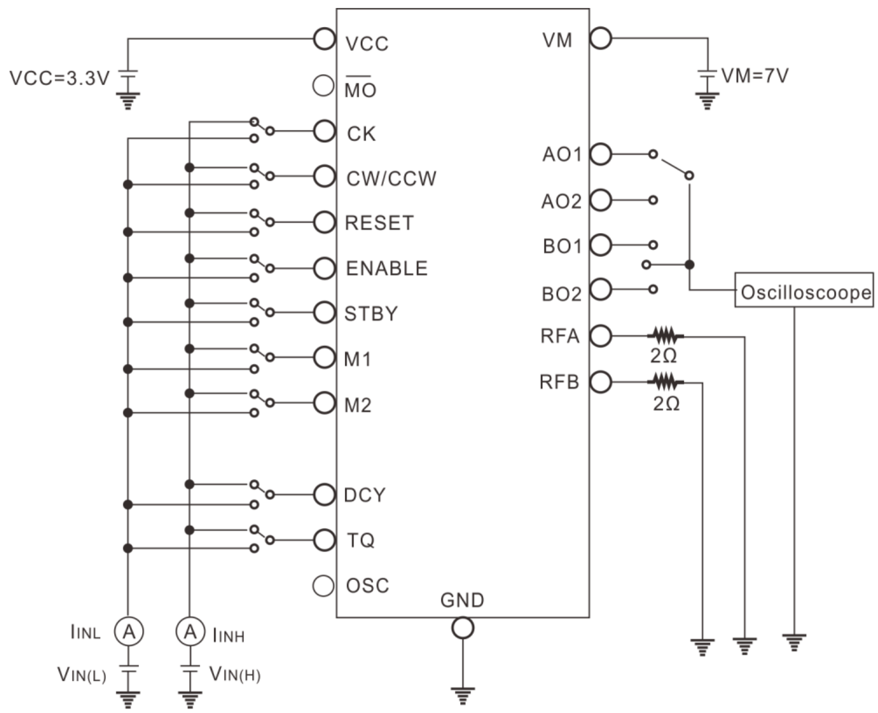
Input Pins	Input Level	Hysteresis
CW/CCW, CK, RESET ENABLE, MI, M2	TTL	Yes
STBY, TQ, DCY	CMOS	No

Parameter				Symbol	Conditions		Min.	Typ.	Max.	Unit	Remark
Output driver RDS(on)				RDS(on)	I_{OUT}= 0.1 A		-	1.8	-	Ω	
					I_{OUT} = 0.6A		-	1.5	-		
Output saturation voltage				$V_{SAT(U+L)}$	I_{OUT}= 0.1 A		-	0.18	0.2	V	
					I_{OUT} = 0.6A		-	0.9	1.3	V	
Diode forward voltage				V_{FU}	I_{OUT} =0.6 A		-	0.95	1.2	V	Fig5
				V_{FL}			-	0.95	1.2	V	
A/B-phase chopping current	2W1-2-phase	W1-2-phase	1-2-phase	Vector	θ =0	TQ: L R_{NF}= 2Ω C_{OSC} = 220pF	-	100	-	%	Fig3
	2W1-2-phase	-	-		θ=1/8		92	98	101		
	2W1-2-phase	W1-2-phase	-		θ= 2/8		86	92	98		
	2W1-2-phase	-	-		θ= 3/8		77	83	89		
	2W1-2-phase	W1-2-phase	1-2-phase		θ= 4/8		65	71	77		
	2W1-2-phase	-	-		θ= 5/8		50	56	62		
	2W1-2-phase	W1-2-phase	-		θ= 6/8		32	38	48		
	2W1-2-phase	-	-		θ= 7/8		14	20	32		
	2-phase excitation				-		-	100	-		-

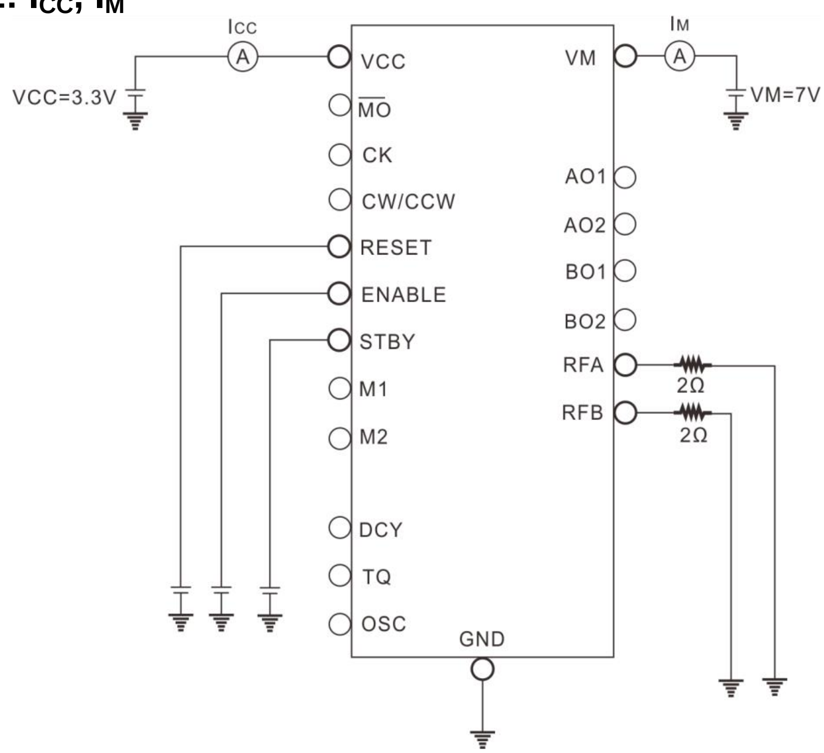
Note: Relative to the peak current at θ = 0.

Parameter		Symbol	Conditions	Min.	Typ.	Max.	Unit	Remark
Output transistor switching characteristics		tr	load: 5mH, 50Ω	-	10	-	ns	Fig7
		tf		-	10	-		
		t_{PLH}	CK to Output	-	400	-		
		t_{PHL}		-	500	-		
		t_{PLH}	RESET to Output	-	400	-		
		t_{PHL}		-	500	-		
		t_{PLH}	ENABLE to Output	-	40	-	ns	
		t_{PHL}L		-	20	-		
Output leakage current	Upper	I_{OH}	V_M = 13V	-	-	1	µA	Fig6
	Lower	I_{OL}		-	-	1		

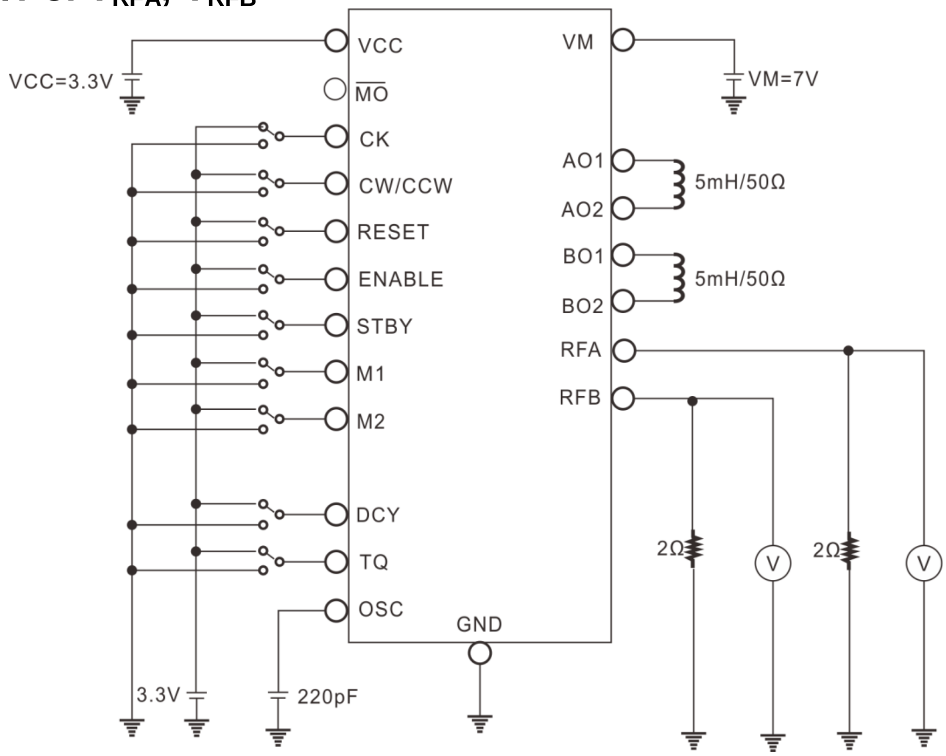
TEST CIRCUIT 1: $V_{IN(H)}$, $V_{IN(L)}$, I_{INH}, I_{INL}



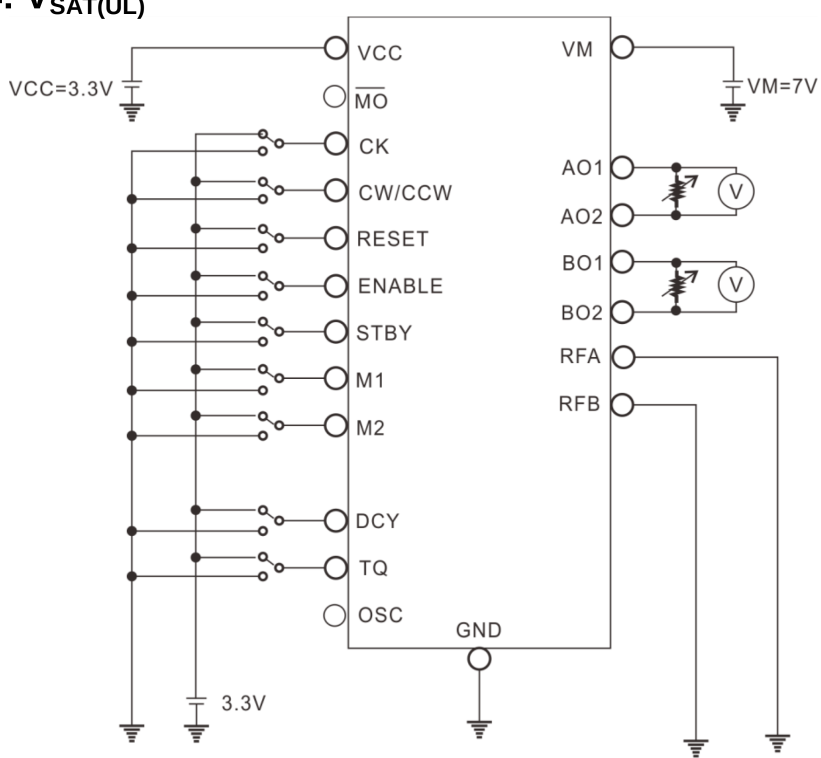
TEST CIRCUIT 2: I_{CC}, I_M



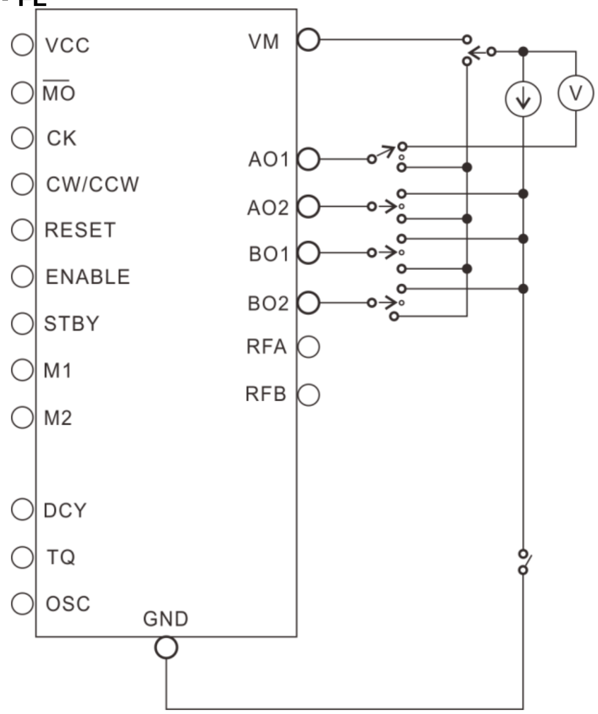
TEST CIRCUIT 3: V_{RFA}, V_{RFB}



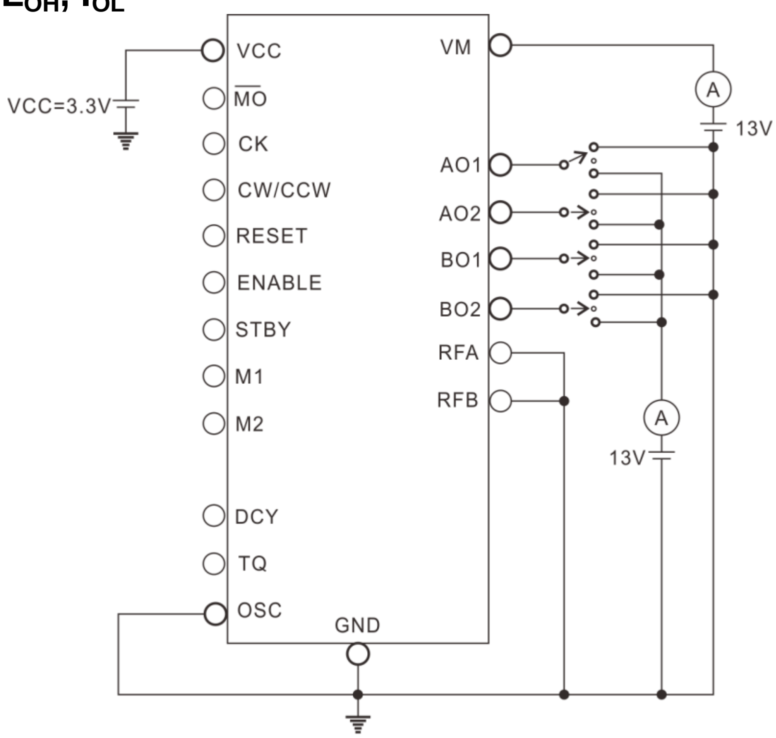
TEST CIRCUIT 4: $V_{SAT(UL)}$



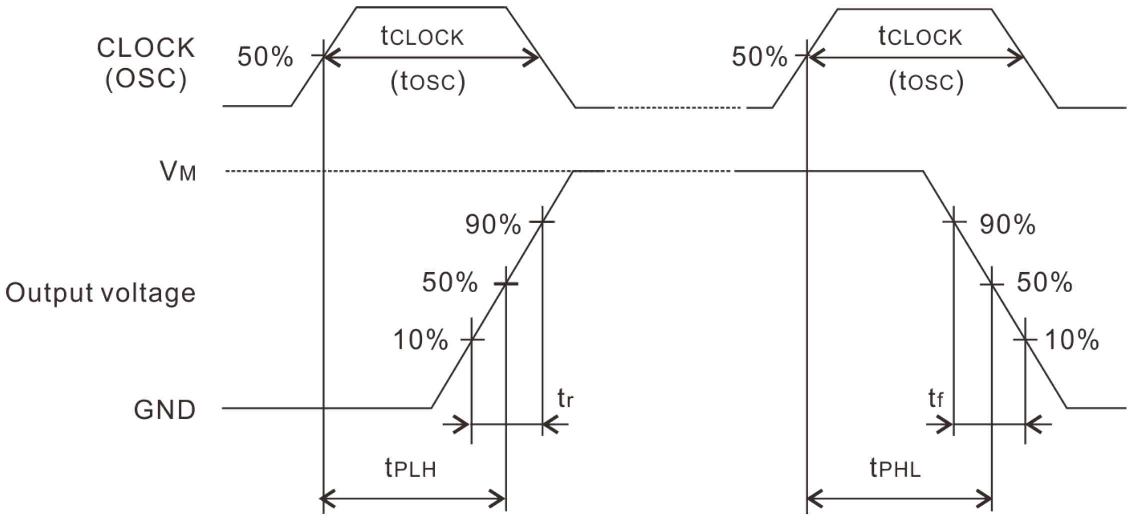
TEST CIRCUIT 5: V_{FU}, V_{FL}



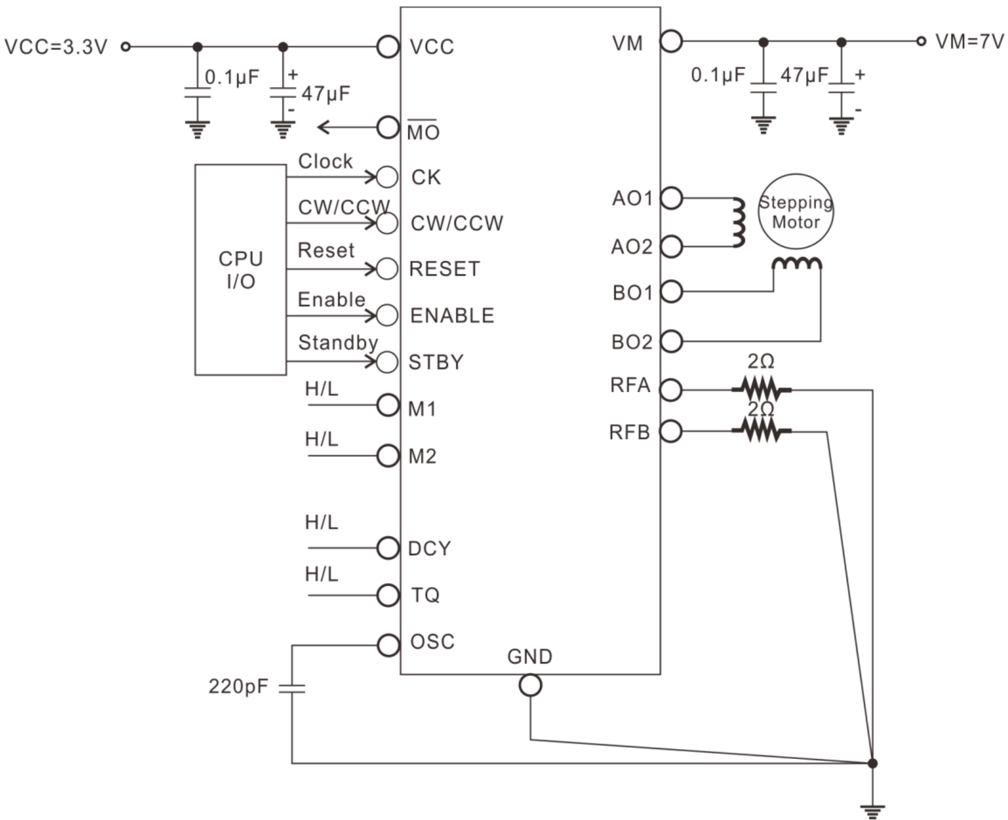
TEST CIRCUIT 6: L_{OH}, I_{OL}



AC ELECTRICAL CHARACTERISTICS, TEST CIRCUIT 7: CK (OSC) AND OUTPUT VOLTAGE



APPLICATION CIRCUIT EXAMPLE

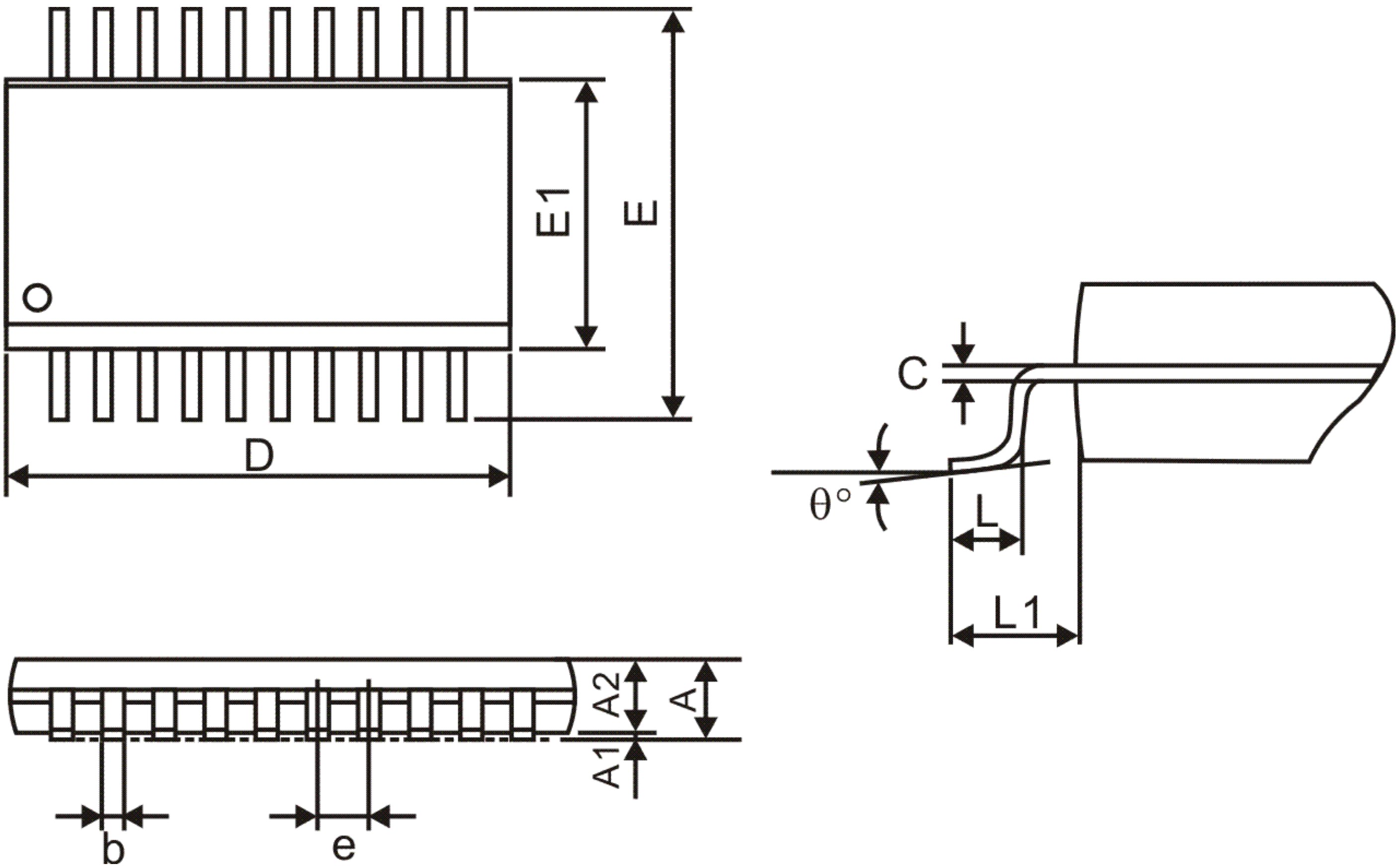


Note 1: Capacitors for the power supply lines should be connected as close to the IC as possible.
Note 2: The STBY pin must be set Low upon powering on and off the device. Otherwise, a large current might abruptly flows through the output pins.
Also, at the power-on, VM must be applied after applying V_{CC}. At the power-off, VCC must be turned off after turning off VM.

Usage Considerations
A large current might abruptly flow through the IC in case of short-circuit across outputs, a short-circuit to power supply or a short-circuit to ground, leading to a damage of the IC. Also, the IC or peripheral parts may be permanently damaged or emit smoke or fire resulting in injury especially if a power supply pin (V_{CC}, $V_{M)}$ or an output pin (AO1, AO2, BO1,BO2) is short-circuited to adjacent or any other pins
.
These possibilities should be fully considered in the design of the output, V_{CC}, V_M and ground lines.
Install this IC correctly. If not, (e.g., installing it in the wrong position,) the IC may be damaged permanently.
Fuses should be connected to the power supply lines.

PACKAGE INFORMATION

TSSOP20 173MIL



Symbol	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	6.40	6.50	6.60
e	0.65 BSC.		
E	6.40 BSC.		
E1	4.30	4.40	4.50
L	0.45	0.60	0.75
L1	1.0 REF.		
θ	0°	-	8°

Notes:
1. Refer to JEDEC MO-153 AC
2. Unit: mm

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REVISION HISTORY

Date	Revision No.	Reference No.	Modification
09/March/2016	PT2465 REF 1.0		Initial issued, V1.2